

FIG. 2A

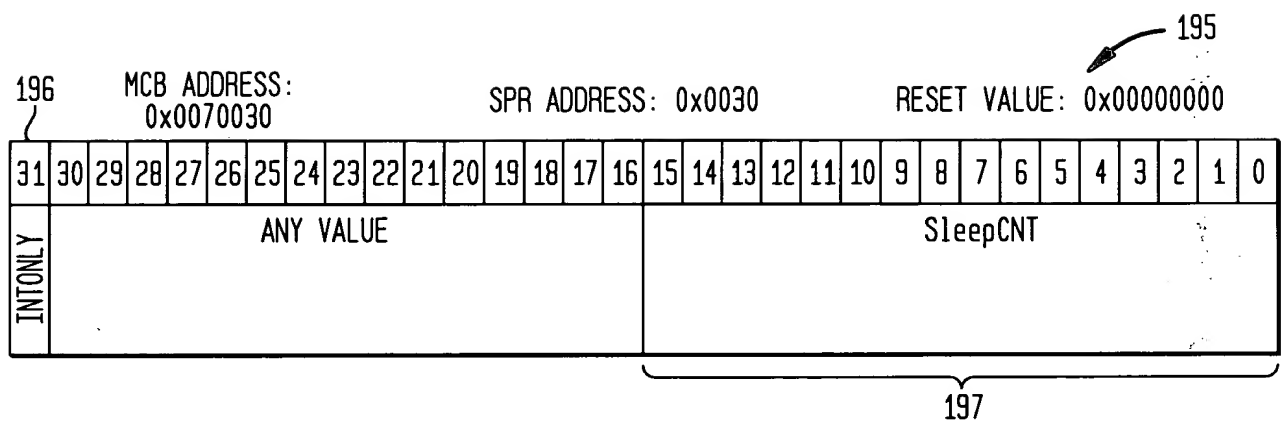


FIG. 2B

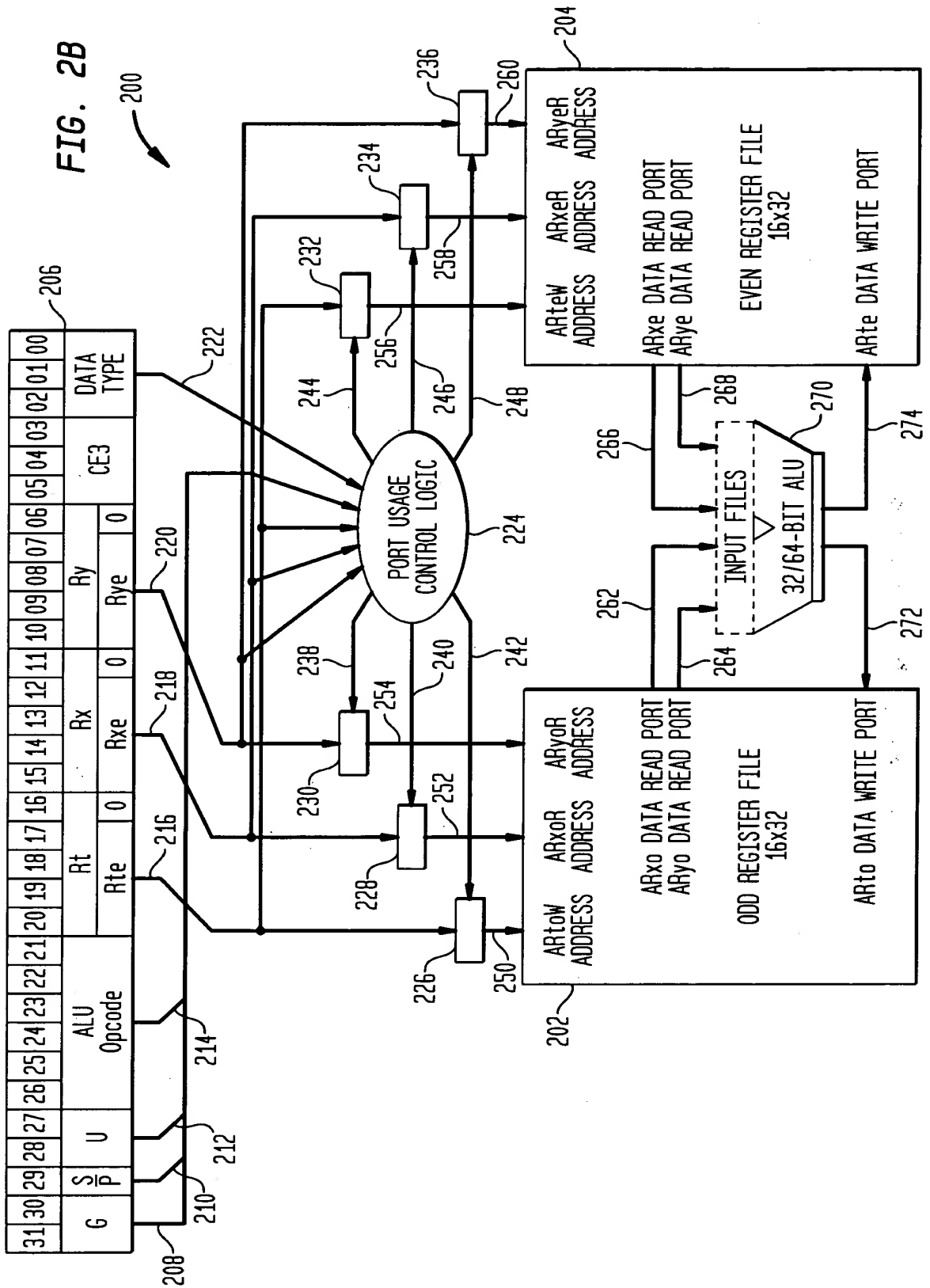


FIG. 3A

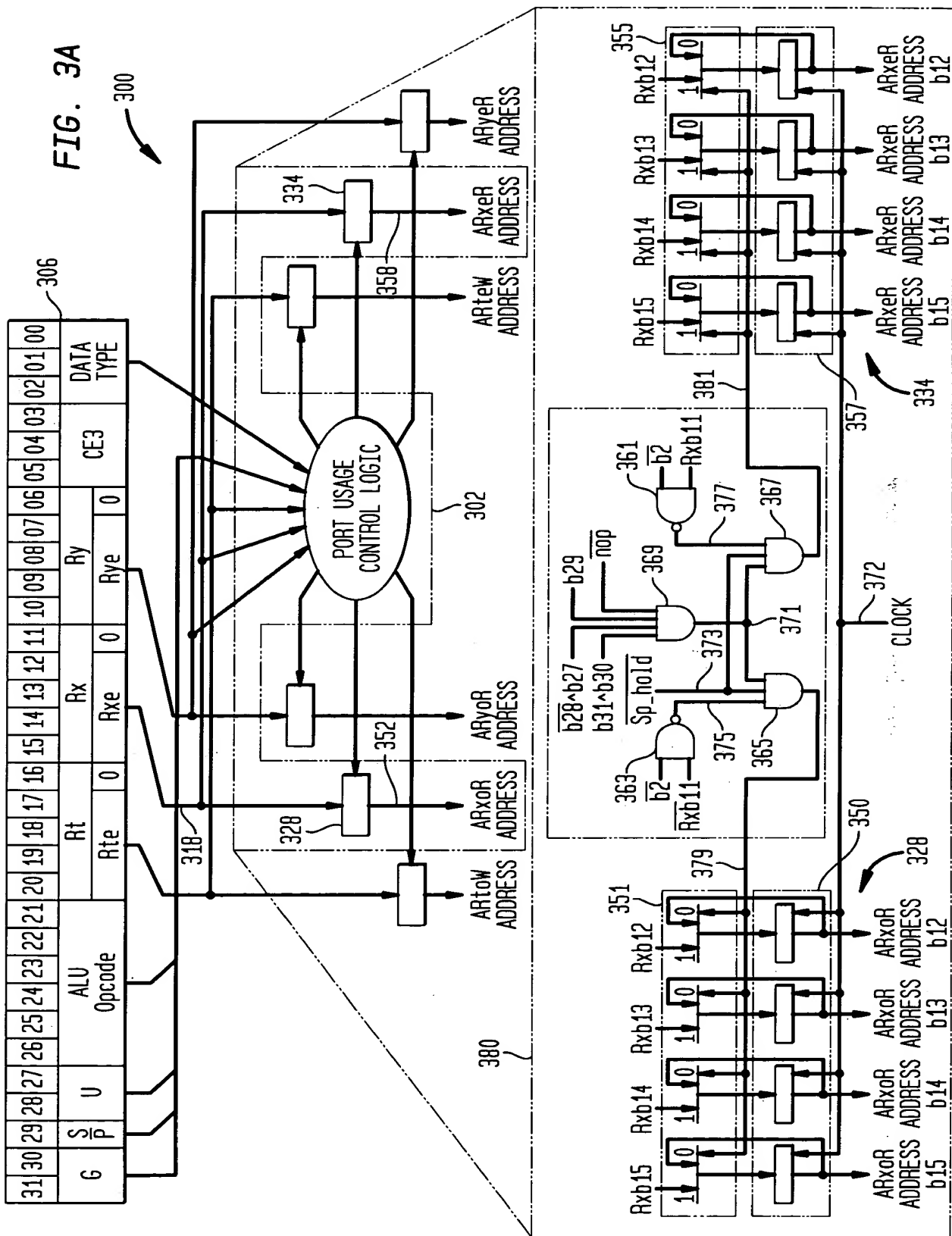


FIG. 3B

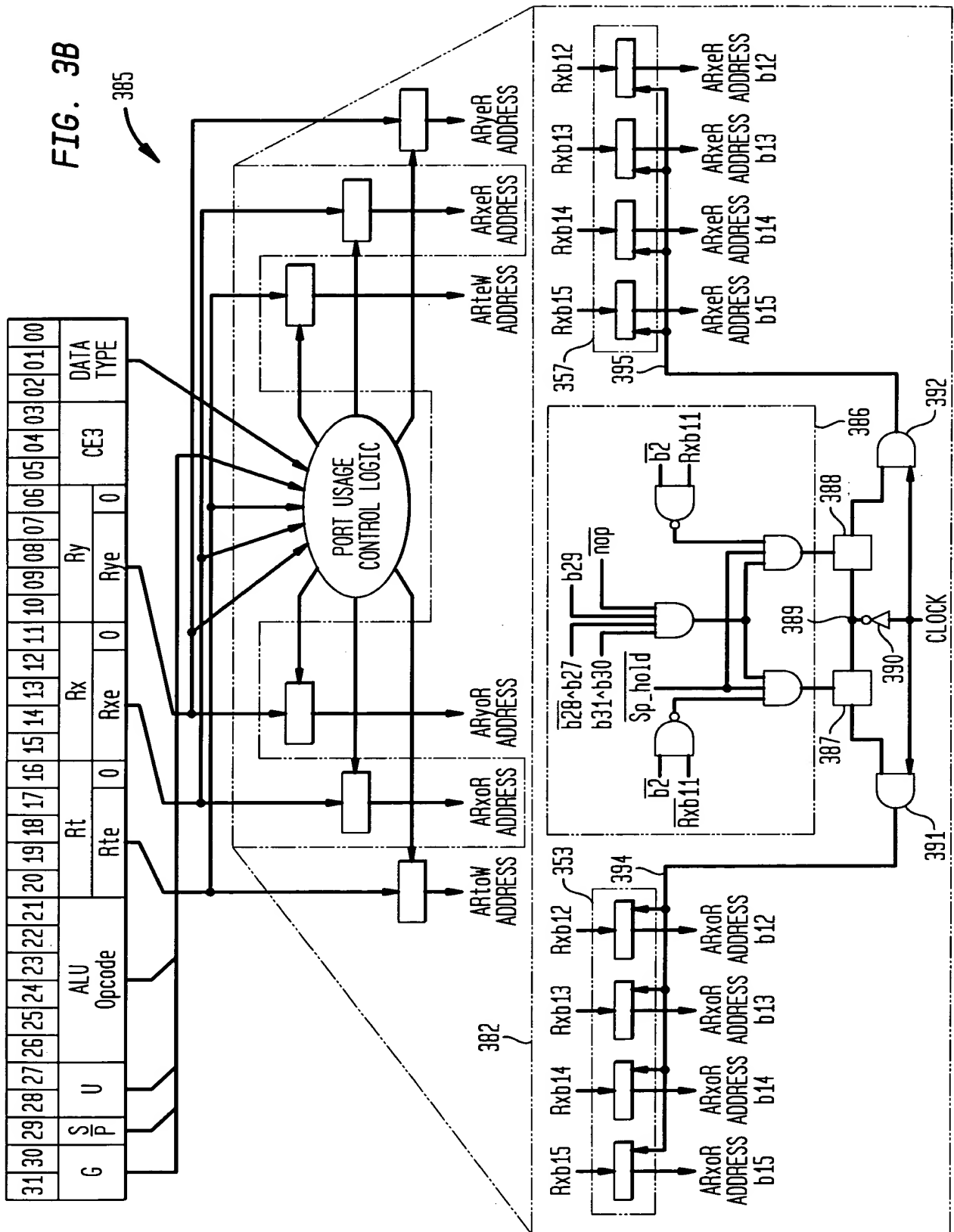


FIG. 4

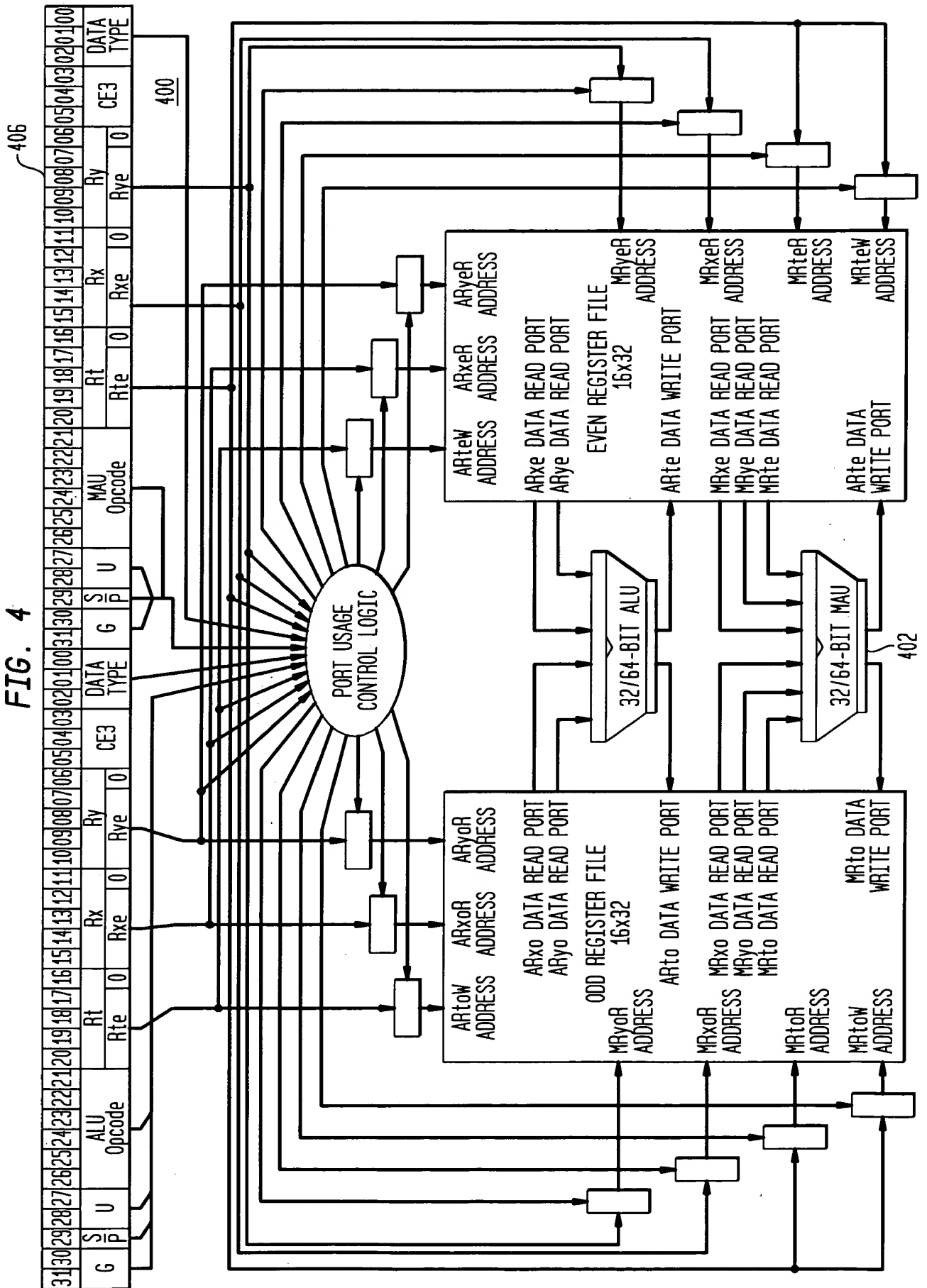
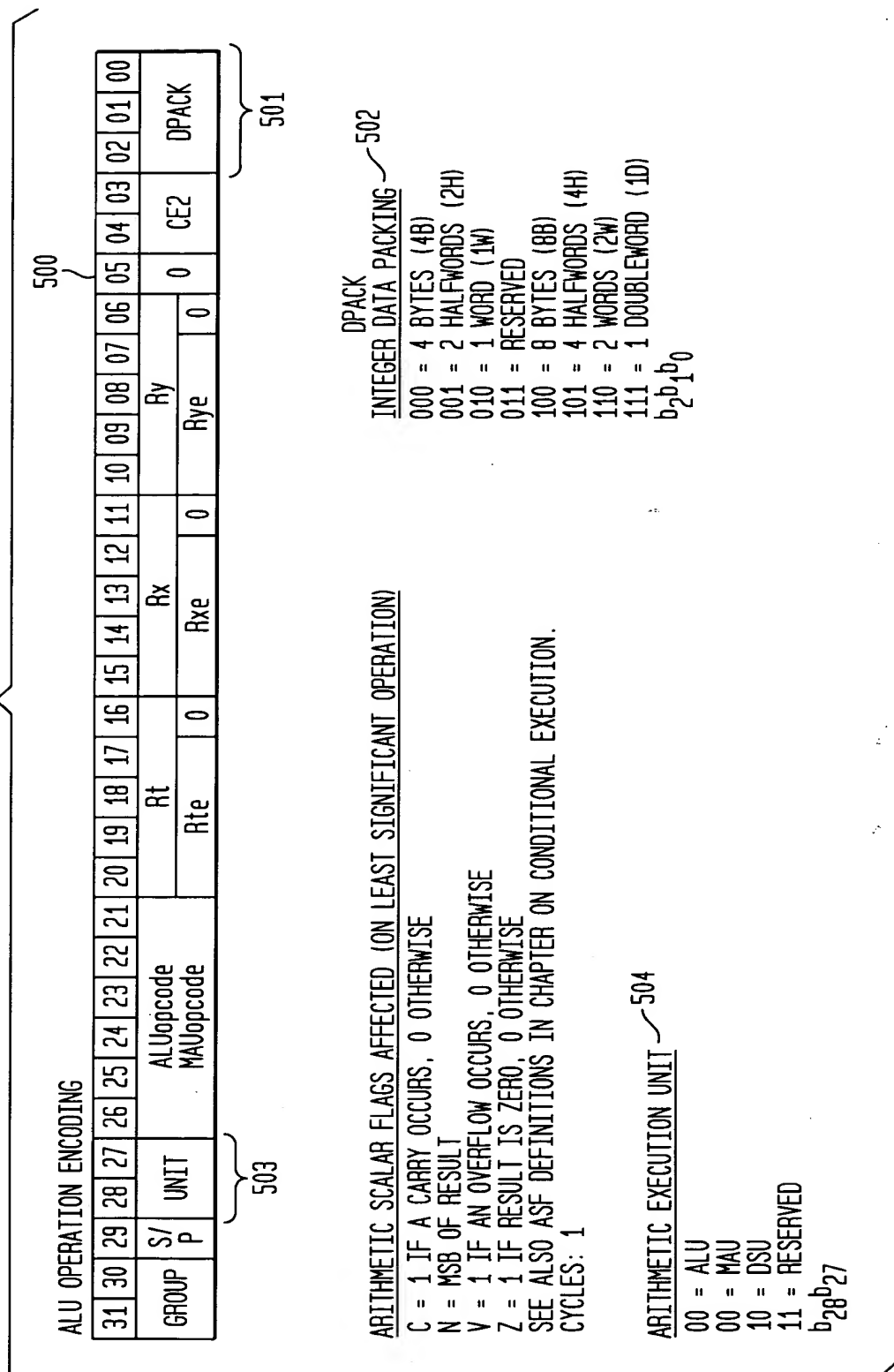


FIG. 5A



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FIG. 5B

DESCRIPTION

THE SUM OF SOURCE REGISTERS Rx AND Ry IS STORED IN TARGET REGISTER Rt.
SYNTAX/OPERATION

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INSTRUCTION	OPERANDS	OPERATION	ACF
DOUBLEWORD			
ADD.[SP][AM].1D	Rte, Rxe, Rye	$Rto \leftarrow Rte \leftarrow Rxo \parallel Rxe + Ryo \parallel Rye$	NONE
[TF].ADD.[SP][AM].1D	Rte, Rxe, Rye	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
WORD			
ADD.[SP][AM].1W	Rt, Rx, Ry	$Rt \leftarrow Rx + Ry$	NONE
[TF].ADD.[SP][AM].1W	Rt, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
DUAL WORDS			
ADD.[SP][AM].2W	Rte, Rxe, Rye	$Rto \leftarrow Rxo + Ryo$ $Rte \leftarrow Rxe + Rye$	NONE
[TF].ADD.[SP][AM].2W	Rte, Rxe, Rye	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
DUAL HALFWORDS			
ADD.[SP][AM].2H	Rt, Rx, Ry	$Rt.H1 \leftarrow Rx.H1 + Ry.H1$ $Rt.H0 \leftarrow Rx.H0 + Ry.H0$	NONE
[TF].ADD.[SP][AM].2H	Rt, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
QUAD HALFWORDS			
ADD.[SP][AM].4H	Rte, Rxe, Rye	$Rto.H1 \leftarrow Rxo.H1 + Ryo.H1$ $Rto.H0 \leftarrow Rxo.H0 + Ryo.H0$ $Rte.H1 \leftarrow Rxe.H1 + Rye.H1$ $Rte.H0 \leftarrow Rxe.H0 + Rye.H0$	NONE
[TF].ADD.[SP][AM].4H	Rte, Rxe, Rye	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
QUAD BYTES			
ADD.[SP][AM].4B	Rt, Rx, Ry	$Rt.B3 \leftarrow Rx.B3 + Ry.B3$ $Rt.B2 \leftarrow Rx.B2 + Ry.B2$ $Rt.B1 \leftarrow Rx.B1 + Ry.B1$ $Rt.B0 \leftarrow Rx.B0 + Ry.B0$	NONE
[TF].ADD.[SP][AM].4B	Rt, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
OCTAL BYTES			
ADD.[SP][AM].8B	Rte, Rxe, Rye	$Rto.B3 \leftarrow Rxo.B3 + Ryo.B3$ $Rto.B2 \leftarrow Rxo.B2 + Ryo.B2$ $Rto.B1 \leftarrow Rxo.B1 + Ryo.B1$ $Rto.B0 \leftarrow Rxo.B0 + Ryo.B0$ $Rte.B3 \leftarrow Rxe.B3 + Rye.B3$ $Rte.B2 \leftarrow Rxe.B2 + Rye.B2$ $Rte.B1 \leftarrow Rxe.B1 + Rye.B1$ $Rte.B0 \leftarrow Rxe.B0 + Rye.B0$	NONE
[TF].ADD.[SP][AM].8B	Rte, Rxe, Rye	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE

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FIG. 6A

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MPYA-MULTIPLY ACCUMULATE
ENCODING

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
GROUP		S/P	UNIT		MAUpcode						Rte		0	Rx				Ry				CE3			MPACK						

FIG. 6B

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SYNTAX/OPERATION

INSTRUCTION	OPERANDS	OPERATION	ACF
WORD			
MPYA.[SP]M.1[SU]W	Rte, Rx, Ry	DO OPERATION BELOW BUT DO NOT AFFECT ACFs	NONE
MPYA[CNVZ].[SP]M.1[SU]W	Rte, Rx, Ry	$Rto \leftarrow Rte \leftarrow Rto \mid Rte + (Rx * Ry)$	F0
[TF].MPYA.[SP]M.1[SU]W	Rte, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN ACFs	NONE
DUAL HALFWORDS			
MPYA.[SP]M.2[SU]H	Rte, Rx, Ry	DO OPERATION BELOW BUT DO NOT AFFECT ACFs	NONE
MPYA[CNVZ].[SP]M.2[SU]H	Rte, Rx, Ry	$Rto \leftarrow Rto + (Rx.H1 * Ry.H1)$ $Rte \leftarrow Rte + (Rx.H0 * Ry.H0)$	F1 F0
[TF].MPYA.[SP]M.2[SU]H	Rte, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN ACFs	NONE
QUAD BYTES			
MPYA.[SP]M.4[SU]B	Rte, Rx, Ry	DO OPERATION BELOW BUT DO NOT AFFECT ACFs	NONE
MPYA.[CNVZ].[SP]M.4[SU]B	Rte, Rx, Ry	$Rto.H1 \leftarrow Rto.H1 + (Rx.B3 * Ry.B3)$ $Rto.H0 \leftarrow Rto.H0 + (Rx.B2 * Ry.B2)$ $Rte.H1 \leftarrow Rte.H1 + (Rx.B1 * Ry.B1)$ $Rte.H0 \leftarrow Rte.H0 + (Rx.B0 * Ry.B0)$	F3 F2 F1 F0
[TF].MPYA.[SP]M.4[SU]B	Rte, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE

FIG. 6C

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ARITHMETIC SCALAR FLAGS AFFECTED
(ON LEAST SIGNIFICANT OPERATION)

C = NOT AFFECTED
 N = MSB OF RESULT
 V = NOT AFFECTED
 Z = 1 IF RESULT IS ZERO,
 0 OTHERWISE
 CYCLES: 2

ARITHMETIC EXECUTION UNIT

00 = ALU
 00 = MAU
 10 = DSU
 11 = RESERVED
 $b_{28}b_{27}$

INSTRUCTION GROUP

00 = RESERVED
 00 = FLOW CONTROL
 10 = LOAD/STORE (LU, SU)
 11 = ARITHMETIC/LOGICAL
 (ALU, MAU, DSU)
 $b_{31}b_{30}$

MPACK-MULTIPLY DATA PACKING

000 = RESERVED
 001 = 2 HALFWORDS (2H)
 010 = 1 WORD (1W)
 011 = RESERVED
 100 = RESERVED
 101 = 4 HALFWORDS (4H)
 FOR MPYH AND MPYL
 110 = RESERVED
 111 = RESERVED
 $b_2b_1b_0$
 SP/PE SELECT
 0 = SP
 1 = PE

ENABLE MASK BITS



RECEIVED 32-BIT XV INSTRUCTION 7



